

(19)



Europäisches Patentamt

European Patent Office

Office européen des brevets



(11)

EP O 751 621 B1

(12)

EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention
of the grant of the patent:
15.04.1998 Bulletin 1998/16

(51) Int Cl.⁶: **H03K 17/06, H03K 17/042**

(21) Application number: **95830283.8**

(22) Date of filing: **30.06.1995**

(54) Bootstrap line power supply regulator with no filter capacitor

Versorgungsspannungsregler für Bootstrableitung ohne Filterkondensator

Régulateur d'alimentation pour ligne bootstrap sans capacité de filtrage

(84) Designated Contracting States:
DE FR GB IT

(43) Date of publication of application:
02.01.1997 Bulletin 1997/01

(73) Proprietor: **SGS-THOMSON
MICROELECTRONICS s.r.l.
20041 Agrate Brianza (Milano) (IT)**

(72) Inventors:
• **Masini, Marco
I-20162 Milano (IT)**

• **Storti, Sandro
I-20099 Sesto S. Giovanni (IT)**
• **Bolocchi, Stefania
I-27012 Certosa (IT)**

(74) Representative: **Cerbaro, Elena et al
STUDIO TORTA S.r.l.,
Via Viotti, 9
10121 Torino (IT)**

(56) References cited:
EP-A- 0 103 645 EP-A- 0 367 006
WO-A-94/27370 DE-A- 3 405 936
US-A- 3 714 466 US-A- 5 111 084

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

Description

The present invention relates to a bootstrap line power supply regulator with no filter capacitor. In particular, the present invention relates to a power supply regulator for a switching-type power stage of the type featuring power MOS transistors and a bootstrap capacitor for biasing the top power transistor at a level higher than the supply voltage.

As is known, a power stage of the above type is supplied with a low-power square-wave signal, supplies a square-wave power output voltage, and typically presents the structure shown in Figure 1 and described below to give a clear idea of the problem underlying the present invention.

The Figure 1 power stage, indicated as a whole by 1, comprises a pair of N-channel power MOS transistors 2, 3 connected between a supply line 4 and a ground line (reference potential line) 5. Transistor 2 (constituting the high-side power transistor) has the drain terminal connected to supply line 4 at potential V_{cc} , and the source terminal connected to an output node 6; and transistor 3 (constituting the low-side power transistor) has the drain terminal connected to output node 6, and the source terminal connected to ground line 5. Power stage 1 is controlled by a drive stage 8 having an input 9 supplied with a low-power square-wave input signal IN, and a pair of outputs 10, 11 connected by respective buffer amplifiers 12, 13 to the gate terminals of transistors 2, 3 respectively. Drive stage 8 is a known type, and, according to one embodiment, for example, comprises an N-channel MOS transistor with the gate terminal supplied with signal IN, the source terminal grounded, and the drain terminal connected to a supply line via a resistor. The drain terminal of the transistor forms output 10, and output 11 is connected directly to input 9.

Buffer amplifier 12 has a first and second bias input 15, 16 connected respectively to nodes 17 and 6; and buffer amplifier 13 has a first and second bias input 18, 19 connected respectively to a regulated-voltage input node 22 and to ground line 5.

Power stage 1 is supplied by a regulated-voltage power supply 21 comprising a voltage source 23 generating a regulated voltage V_{REG} and connected between regulated-voltage node 22 and ground, and a diode 24 with its anode terminal connected to node 22 and its cathode terminal connected to node 17. Figure 1 also shows a bootstrap capacitor 25 connected between nodes 17 and 6, for charging high-side power transistor 2.

Figure 1 also shows a filter capacitor 26 connected parallel with voltage source 23; a parasitic capacitor 27 associated and connected parallel with diode 24; and the protection diodes (not numbered in detail) associated in known manner with the power MOS transistors.

Ignoring filter capacitor 26 and parasitic capacitor 27 for the time being, the Figure 1 circuit operates as follows. On the basis of input signal IN at input 8, drive

stage 9 generates, at outputs 10, 11, two complementary square-wave signals for driving buffer amplifiers 12, 13, which in turn generate gate voltages related to the voltages at their terminals 16, 19, and such as to alternatively turn on transistors 2, 3, and ensure the necessary source-gate voltage drop for achieving a good saturation level of transistors 2, 3.

More specifically - assuming that, when signal IN is high, output 10 of the drive stage is high and output 11 is low, and vice versa - when IN is low, output 11 is at a high voltage; the output of buffer amplifier 13 is high (roughly 10-15 V with respect to ground); transistor 3 is saturated and grounds output node 6 (OUT output low); conversely, the output of buffer amplifier 12 is low; transistor 2 is off; node 22 is at a higher potential than node 6; and diode 24 is biased directly to charge bootstrap capacitor 25 to regulated voltage V_{REG} (less the voltage drop across diode 24).

When signal IN switches to high, output 11 of drive stage 8 switches to a low voltage; the output of buffer amplifier 13 is at ground potential so that transistor 3 is turned off; conversely, output 10 switches to high and turns on transistor 2, so that output node 6 increases in voltage; as soon as the OUT voltage at node 6 increases, the voltage at node 17 also increases by virtue of bootstrap capacitor 25, and diode 24 becomes off. In other words, an increase in the voltage at output node 6 is accompanied by a corresponding increase in the voltage at node 17, so that the output voltage supplied by buffer amplifier 12 and related to node 6, i.e. to the source terminal of transistor 2, is such as to fully saturate transistor 2 and so bring node 6 to a high voltage (OUT output equal to V_{cc}).

In practice, as the output signal OUT switches from low (ground) to high (V_{cc}), bootstrap capacitor 25, via buffer amplifier 12, supplies the gate terminal of high-side transistor 2 with the necessary charge, and recharges itself when the OUT output is low. In the first step, current flows from regulated-voltage source 23 through diode 24 to bootstrap capacitor 25; in the second step, current flows from bootstrap capacitor 25 to node 17, input 15 of buffer amplifier 12, the gate terminal of transistor 2, node 6, and back to bootstrap capacitor 25, and diode 24 is inversely biased with no current flowing through it.

In the event the output voltage OUT switches to high before bootstrap capacitor 25 is fully charged, the Figure 1 circuit encounters problems in that, in this case, diode 24 is still supplied with the charge current I of capacitor 25, and has therefore accumulated a minority charge $Q = I \tau$ wherein τ is the transit time of the minority carriers. Thus, account must now be taken of the parasitic capacitor indicated by 27 in Figure 1, and presenting a diffusion capacitance $C_d = Q/V_t$ wherein V_t is the thermal voltage. This therefore results in a capacitive network comprising bootstrap capacitor 25 and parasitic capacitor (diffusion capacitance) 27, and which tends to transmit the transition at the output to source V_{REG} , and so

generate a current spike I_{sp} in voltage source 23.

To roughly calculate the value of current I_{sp} , diode 24 must lose the minority charge Q in time Δt , wherein Δt is the fraction of the transition time of output voltage OUT required to switch diode 24 from a direct to an inverse bias, so that $I_{sp} = Q/\Delta t$.

For output voltage OUT switching times of about 100 ns, fraction Δt may be around 10 ns or less; and, if, for example, $I = 200$ mA and $\tau = 20$ ns, current spike I_{sp} entering source 23 is around 400 mA or even more.

Given the inductive nature of the output impedance of a power supply regulator, the current spike causes an unacceptable, uncontrolled increase in the regulated voltage at node 22.

To solve the problem, it has been proposed to use a filter capacitor - indicated by 26 in Figure 1 - connected parallel with regulated-voltage source 23, and which presents a capacitance of about one nanofarad, and absorbs the current spike with no appreciable increase in voltage at its terminals (and hence at node 22).

The disadvantage of this solution lies in the above capacitance preventing integration of filter capacitor 26 which thus represents an additional external component.

WO-A-94/27370 describes a power supply regulator, wherein, in order to eliminate discrete components such as the bootstrap capacitor and the diode, an on-chip circuit emulating the diode is disclosed. The emulating circuit comprises an LDMOS transistor and a drive circuitry to switch on the LDMOS transistor when the lower power transistor of the driver is on and to switch off the LDMOS transistor in the opposite phase.

It is an object of the present invention to provide a power supply regulator of the above type, designed to operate correctly in any situation, even in the absence of a filter capacitor.

According to the present invention, there is provided a bootstrap line power supply regulator as claimed in Claim 1.

In practice, according to one aspect of the present invention, the diode interposed between the bootstrap capacitor and the regulated-voltage source is turned off before the voltage at the low terminal of the capacitor (connected to the output of the power stage) switches from low to high.

A preferred embodiment of the present invention will be described by way of example with reference to the accompanying drawings, in which:

Figure 1 shows a diagram of a switching-type power stage comprising a bootstrap capacitor and a known power supply regulator;

Figure 2 shows an overall diagram of the power supply regulator according to the present invention, and as applied to the Figure 1 power stage;

Figure 3 shows plots of a number of voltages relative to the Figure 2 diagram;

Figure 4 shows a more detailed circuit diagram of a

possible implementation of the Figure 2 arrangement.

In Figure 2, the power supply regulator is indicated by 30, and is applied to a power stage 1 of the type shown in and described in detail with reference to Figure 1. The Figure 2 components similar to those in Figure 1 are therefore indicated using the same reference numbers with no further description.

In addition to regulated-voltage source 23, the Figure 2 power supply regulator 30 also comprises an inverting buffer amplifier 31 in turn comprising a signal input 32 connected to input 9 of drive stage 8 to receive the same IN signal, and two bias inputs 33, 34, of which input 33 is connected to node 22 set at regulated voltage V_{REG} , and input 34 is grounded. The output of inverting buffer amplifier 31 defines a node 36 (set at a switched regulated voltage V_{36}) connected to the anode of diode 24, the cathode of which is connected, as in Figure 1, to node 17 to charge bootstrap capacitor 25.

Operation of the circuit according to the present invention is based on the fact that, as regards the downstream power stage 1, the value of regulated voltage V_{REG} is only of importance when output 6 of the power stage is low, i.e. when bootstrap capacitor 25 is being charged, whereas, when output 6 is high, the regulated voltage value is no longer of any importance by virtue of buffer amplifier 12 being supplied by bootstrap capacitor 25; and on the fact that, to prevent current spikes from being transmitted to regulated-voltage source 23, diode 24 need simply be turned off before output 6 of power stage 1 switches to high.

The Figure 2 circuit therefore operates as follows. When the input signal is low (0 V), output 11 of drive stage 8 and the output of buffer amplifier 13 are high, so that transistor 3 is turned on; conversely, the output of buffer amplifier 12 is low, and transistor 2 is turned off, as already described with reference to Figure 1. As such, the output of inverting buffer 31 is high and equal to the regulated voltage V_{REG} at node 22, thus permitting capacitor 25 to be charged to regulated voltage V_{REG} as in the Figure 1 circuit.

When input signal IN switches to high (e.g. 12 V), the output of inverting buffer 31 switches rapidly to ground potential (0 V) and inversely biases diode 24 which is turned off. Following a delay due to switching of drive stage 8, outputs 10, 11 of the drive stage and hence the outputs of buffer amplifiers 12, 13 also switch as described with reference to Figure 1, so that transistor 3 is turned off, and transistor 2 is turned on to connect output terminal 6 to supply voltage V_{cc} when diode 24 is already definitely turned off. Consequently, when output 6 switches, current is prevented from flowing through diode 24 to regulated-voltage source 23, even in the event capacitor 25 is not fully charged.

When input signal IN again switches to low, the regulated voltage at the anode of diode 24 is restored before the OUT output switches to low, thus ensuring boot-

strap capacitor 25 is charged.

The time relationship between the switching of input signal IN, output voltage OUT, and the switched regulated voltage V_{36} at node 36 (anode of diode 24) is shown clearly in the time plots of the three quantities in Figure 3. In particular, following low-to-high switching of input signal IN at instant t_0 , the switched regulated voltage V_{36} switches to low at instant t_1 (turning off inverse-biased diode 24), and output voltage OUT switches to high at instant $t_2 > t_1$.

The time sequence shown (wherein switched regulated voltage V_{36} switches in advance of output voltage OUT) is ensured by the propagation of the IN signal from input 9 to node 36 involving a small number of components (only inverting buffer 34), whereas propagation of the IN signal from input 9 to output 6 involves drive stage 8 (which in itself presents a propagation delay of other than zero), buffer amplifiers 12, 13, and power transistors 2, 3. Moreover, the circuit may be so designed as to ensure that, in any condition, the output always switches after switched regulated voltage V_{36} . For circuits of the type shown, the delay between input 9 and output 6 is typically of about 100 ns, and the delay between input 9 and node 36 may be guaranteed below 50 ns at all times.

One embodiment of the Figure 2 circuit is shown in Figure 4, which shows regulated-voltage source 23 and inverting buffer amplifier 31 in more detail.

More specifically, regulated-voltage source 23 comprises a current source 40 connected between supply line 4 at V_{cc} and the collector of a diode-connected NPN bipolar transistor 41 (with the collector and base short-circuited). The emitter of transistor 41 is connected to the emitter of a diode-connected PNP transistor 42, the collector of which is grounded via two Zener diodes 43, 44 in series with each other. The base terminal of transistor 42 is connected to the base terminal of a PNP transistor 45, the collector of which is grounded, and the emitter of which defines node 22 at regulated voltage V_{REG} . Node 22 is also connected to the emitter of an NPN transistor 46, the base terminal of which is connected to the base terminal of transistor 41, and the collector terminal of which is connected to supply line 4.

Node 22 is also connected to the base terminal of an NPN transistor 49, the collector terminal of which is connected to supply line 4, and the emitter terminal of which is connected to input 18 of buffer amplifier 13 and to a current source 50 interposed between transistor 49 and ground.

Node 22 is also connected to the drain terminal of a P-channel MOS transistor 51, the gate terminal of which is connected to a node 52 defined by the output of a buffer amplifier 53, the input of which is connected to input 9 of drive stage 8 and is supplied with signal IN. Node 52 is also connected to the gate terminal of two N-channel MOS transistors 54 and 55. More specifically, the source terminal of MOS transistor 54 is grounded, and the drain terminal is connected to the drain terminal

of MOS transistor 51; and the source terminal of MOS transistor 55 is also grounded, and the drain terminal is connected to node 36 (anode of diode 24). Finally, node 36 is connected to the emitter of an NPN bipolar transistor 58, the base terminal of which is connected to node 52, and the collector terminal of which is connected to supply line 4.

In Figure 4, too, power MOS transistors 2, 3, 54, 55 are shown together with respective protection diodes (not numbered).

In the Figure 4 circuit, Zener diodes 43, 44 generate the regulated voltage which, added to voltage drop V_{BE} at the base-emitter junction of transistor 41, is supplied to low-output-impedance node 22. Via transistor 49, the regulated voltage (corresponding to V_{REG} in Figure 2) is supplied to buffer amplifier 18; and the same regulated voltage (added to the base-emitter voltage drop V_{BE} of transistor 58 and to the source-drain voltage drop of MOS transistor 51, which is nevertheless substantially negligible) is supplied to node 36 via the inverter formed by MOS transistors 51, 54, 55 when MOS transistor 51 is turned on, to generate the switched regulated voltage V_{36} supplied to diode 24. More specifically, when input signal IN is low, the output of buffer amplifier 53 is also low, so that transistor 51 stays on and transistors 54, 55 stay off; the base terminal of transistor 58 is biased substantially at the regulated voltage at node 22, and supplies the regulated voltage (less voltage drop V_{BE}) to the anode of diode 24 to charge capacitor 25.

When input signal IN switches to high, the output of buffer amplifier 53 also switches to high, thus turning off MOS transistor 51 and turning on MOS transistors 54, 55, which ground node 36, so that diode 24 is turned off as described with reference to Figure 2.

In the Figure 4 circuit also, the propagation delay of the switching edges of input signal IN through buffer amplifier 53 and transistors 51, 58, 54, 55 is less than that of the same edges through components 8, 12, 13, 2, 3, to ensure correct operation of the switched power supply regulator.

The advantages of the circuit described are as follows. Firstly, it provides for preventing uncontrolled variations in the regulated voltage, without using filter capacitors of non-integratable value. Secondly, it involves only a small number of simple, easily-integratable additional components, and therefore practically no increase in manufacturing cost as compared with known circuits. And, thirdly, it is reliable and accurately controlled.

Claims

1. A bootstrap line power supply regulator comprising a regulated voltage source (23) defining a regulated voltage node (22) at a regulated voltage (V_{REG}); a bootstrap capacitor (25) interposed between a supply node (17) and a reference node (6), said reference node (6) being at a reference voltage (OUT)

switchable between a first and a second value, said first value being lower than said second value; and a diode (24) having an anode terminal connected to said regulated voltage node (22) and a cathode terminal connected to said supply node (17); characterized in that it comprises a turn-off means (31) interposed between said regulated voltage node (22) and said anode terminal of said diode (24) for alternately connecting said anode terminal of said diode to a voltage lower than said second value of said reference voltage before said reference voltage switches from said first to said second value and for connecting said anode terminal to said regulated voltage node (22) upon said reference voltage switching from said second to said first value.

2. A power supply regulator according to claim 1, characterized in that it comprises a drive stage (8) having an input (9) supplied with a digital control signal (IN) and an output (10, 11) connected to said reference node (6) and in that said turn-off means comprises a buffer amplifier (31) having an input (32) connected to said input (9) of said drive stage, an output (36) connected to said anode terminal of said diode (24) and at least one bias terminal (33) connected to said regulated voltage node (22).
3. A power supply regulator according to claim 2, characterized in that said buffer amplifier (31) comprises an input buffer (53) and an inverter (51, 54, 55) connected to the output (52) of said input buffer.
4. A power supply regulator according to any of the preceding claims, characterized in that it comprises a power stage (1) including a first and a second power transistor (2, 3) connected between a supply voltage line (4) and a ground line (5) and defining said reference node (6).

Patentansprüche

1. Ein Versorgungsspannungsregler für Bootstrappleitung, der umfaßt eine geregelte Spannungsquelle (23), die einen geregelten Spannungsknoten (22) bei einer geregelten Spannung (V_{REG}) festlegt; einen Bootstrapkondensator (25), der zwischen einem Versorgungsspannungsknoten (17) und einem Bezugsknoten (6) eingefügt ist, wobei der genannte Bezugsknoten (6) auf einer Bezugsspannung (AUS) ist, die zwischen einem ersten und einem zweiten Wert umschaltbar ist, wobei der genannte erste Wert niedriger als der genannte zweite Wert ist; und eine Diode (24), die eine Anodenklemme, die mit dem genannten geregelten Spannungsknoten (22) verbunden ist, und eine Kathodenklemme aufweist, die mit dem genannten Versorgungsspannungsknoten (17) verbunden ist; dadurch gekenn-

zeichnet, daß sie eine Ausschalteneinrichtung (31) umfaßt, die zwischen dem genannten geregelten Spannungsknoten (22) und der genannten Anodenklemme der genannten Diode (24) eingefügt ist, um die genannte Anodenklemme der genannten Diode mit einer Spannung, die niedriger als der genannte zweite Wert der genannten Bezugsspannung ist, zu verbinden, bevor die genannte Bezugsspannung von dem genannten ersten auf den genannten zweiten Wert schaltet, und die genannte Anodenklemme mit dem genannten geregelten Spannungsknoten (22) zu verbinden, wenn die genannte Bezugsspannung von dem genannten zweiten auf den genannten ersten Wert schaltet.

2. Ein Versorgungsspannungsregler gemäß Anspruch 1, dadurch gekennzeichnet, daß er eine Treiberstufe (8) umfaßt, die einen Eingang (9), dem ein digitales Steuersignal (EIN) zugeführt wird, und einen Ausgang (10, 11) aufweist, der mit dem genannten Bezugsknoten (6) verbunden ist, und daß die genannte Ausschalteneinrichtung einen Pufferverstärker (31) umfaßt, der einen Eingang (32), der mit dem genannten Eingang (9) der genannten Treiberstufe verbunden ist, einen Ausgang (36), der mit der genannten Anodenklemme der genannten Diode (24) verbunden ist, und wenigstens eine Vorspannungsklemme (33) aufweist, die mit dem genannten geregelten Spannungsknoten (22) verbunden ist.
3. Ein Versorgungsspannungsregler gemäß Anspruch 2, dadurch gekennzeichnet, daß der genannte Pufferverstärker (31) einen Eingangspuffer (53) und eine Umkehrschaltung (51, 54, 55) umfaßt, die mit dem Ausgang (52) des genannten Eingangspuffers verbunden ist.
4. Ein Versorgungsspannungsregler gemäß irgendeinem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß er eine Leistungsstufe (1) umfaßt, die einen ersten und einen zweiten Leistungstransistor (2, 3) enthält, die zwischen einer Versorgungsspannungsleitung (4) und einer Masseleitung (5) verbunden sind und den genannten Bezugsknoten (6) festlegen.

Revendications

1. Régulateur d'alimentation pour ligne de type à autoélévation comprenant une source de tension régulée (23) définissant un noeud de tension régulée (22) à une tension régulée (V_{REG}); une capacité d'autoélévation (25) interposée entre un noeud d'alimentation (17) et un noeud de référence (6), le dit noeud de référence (6) étant à une tension de référence (OUT) pouvant être commutée entre une première et une seconde valeur, ladite première va-

leur étant inférieure à ladite seconde valeur; et une diode (24) présentant une borne d'anode connectée audit noeud de tension régulée (22) et une borne de cathode connectée audit noeud d'alimentation (17); caractérisé en ce qu'il comprend un moyen de désactivation (31) interposé entre ledit noeud de tension régulée (22) et ladite borne d'anode de ladite diode (24) afin de connecter de manière alternée ladite borne d'anode de ladite diode à une tension inférieure à ladite seconde valeur de ladite tension de référence avant que ladite tension de référence ne commute de ladite première à ladite seconde valeur et afin de connecter ladite borne d'anode audit noeud de tension régulée (22) lors de la commutation de ladite de tension de référence entre ladite seconde et ladite première valeur.

2. Régulateur d'alimentation selon la revendication 1, caractérisé en ce qu'il comprend un étage d'attaque (8) présentant une entrée (9) recevant un signal de commande numérique (1N) et une sortie (10, 11) connectée audit noeud de référence (6) et en ce que ledit moyen de désactivation comprend un amplificateur d'adaptation (31) présentant une entrée (32) connectée à ladite entrée (9) dudit étage d'attaque, une sortie (36) connectée à ladite borne d'anode de ladite diode (24) et au moins une borne de polarisation (33) connectée audit noeud de tension régulée (22).
3. Régulateur d'alimentation selon la revendication 2, caractérisé en ce que ledit amplificateur d'adaptation (31) comprend un adaptateur d'entrée (53) et un inverseur (51, 54, 55) connecté à la sortie (52) dudit adaptateur d'entrée.
4. Régulateur d'alimentation selon l'une quelconque des revendications précédentes, caractérisé en ce qu'il comprend un étage de puissance (1) comprenant un premier et un second transistor de puissance (2, 3) connectés entre une ligne de tension d'alimentation (4) et une ligne de masse (5) et définissant ledit noeud de référence (6).

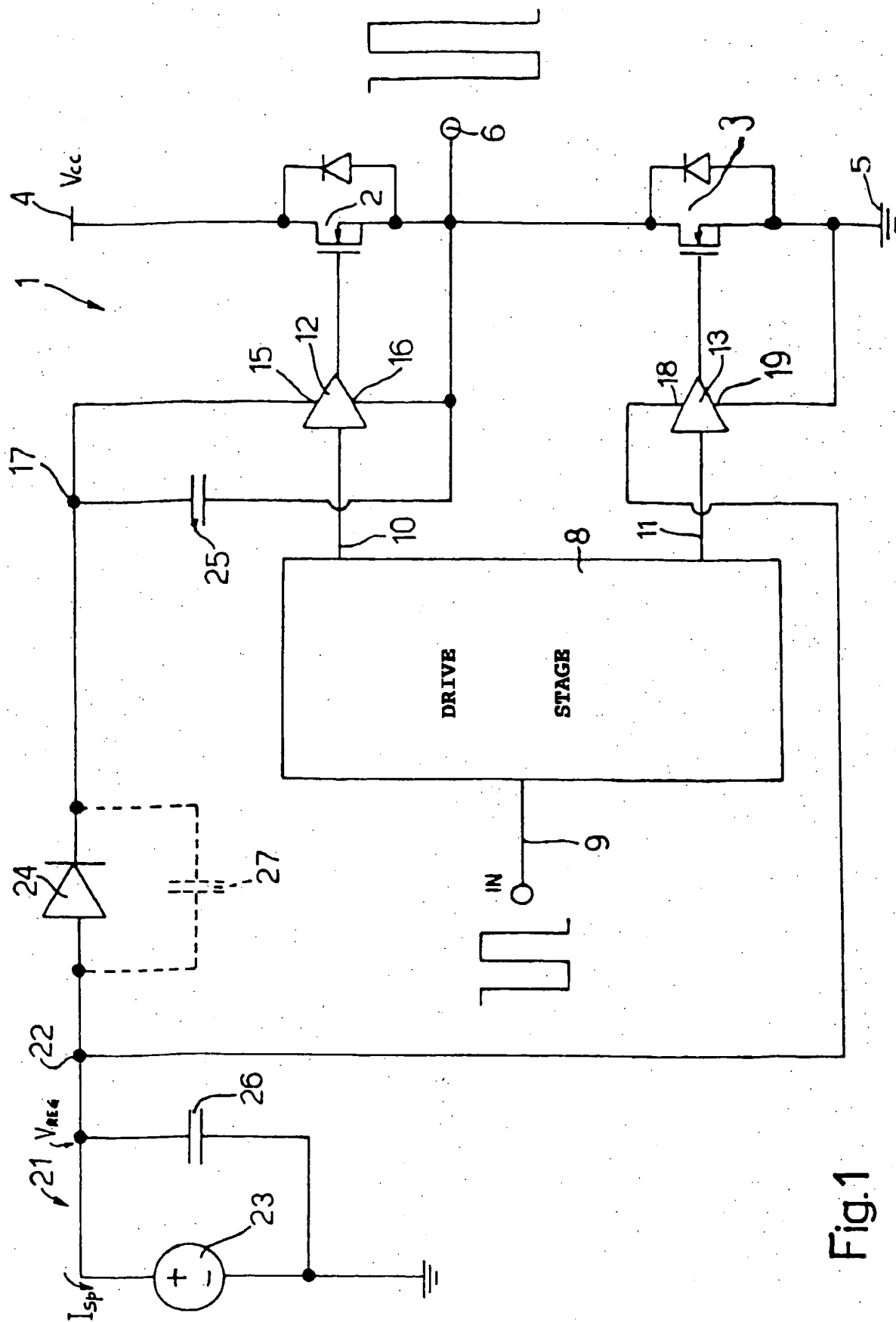
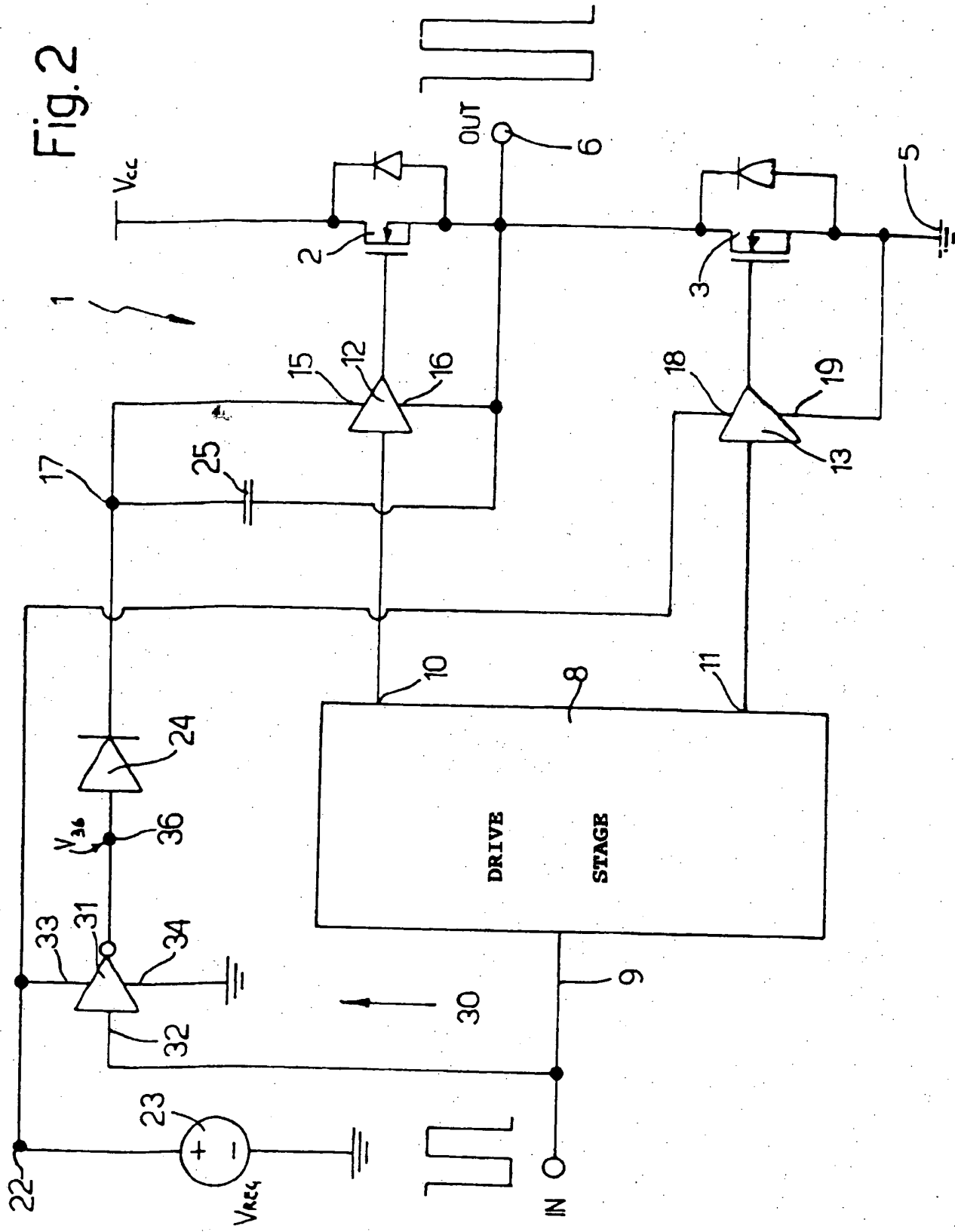


Fig.1

Fig. 2



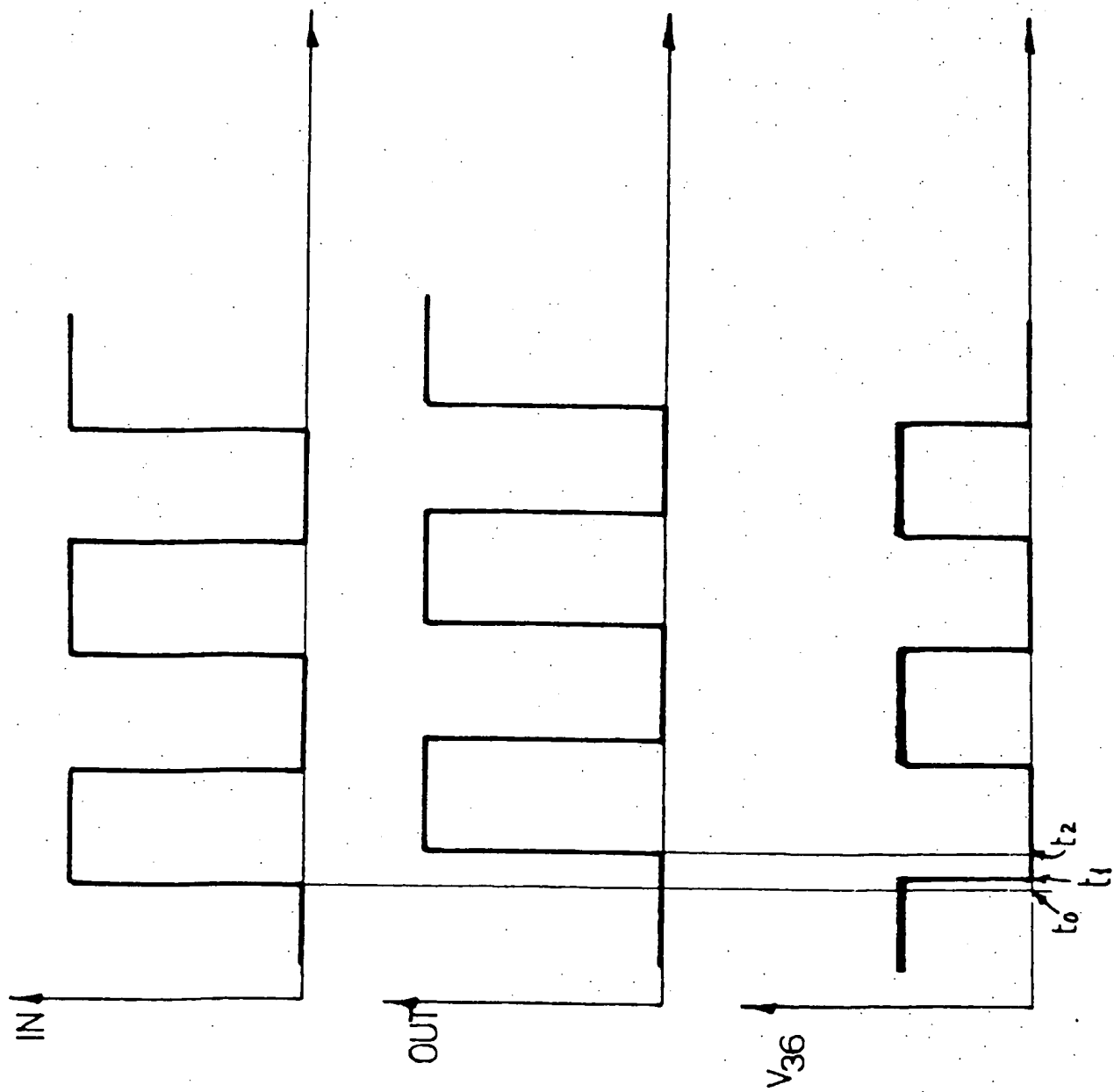


Fig. 3

Fig. 4

